Cascaded DC-DC Converter Systems: Stability Criteria and Solutions

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Outlines

- Backgrounds
- General Impedance-Based Stability for Cascaded System
- Input Impedance Regulation for Load Converter
- Adaptive Impedance Adaptor
- Conclusions
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Centralized Power System vs DPS

Centralized Power System

- Poor cross-regulation;
- Poor dynamic response;
- Large loss due to long distance between the power supply and load.

Distributed Power System

- Modular design;
- Tight regulation of each output.
- Lower loss in the transmission line.
Applications of Distributed Power System

- More-Electric- and All-Electric Aircrafts
- Aerospace Stations
- Warships
- Personal Computer
- Electric Vehicle
- Server
Issues of Cascaded DC-DC Converter System

A Typical Distributed Power System

System stability criterion?

Solutions to improve system stability?
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The above two stability criteria is **contradictory.**


Limitations of the Existing Stability Criteria

The bidirectional converter is a source converter or a load converter?

All the source converters control the intermediate bus voltage. How to obtain the output impedance?
Classifications of Converters: BVCC and BCCC

- **Bus Voltage Controlled Converter (BVCC)**
  - Directly control $v_{bus}$, or
  - Indirectly control $v_{bus}$ by regulating the power.

- **Bus Current Controlled Converter (BCCC)**
  - Directly control $i_{bus}$, or
  - Indirectly control $i_{bus}$ by regulating the power.

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**Diagram:**

- **PV or Wind Turbine**
- **Storage Unit**
- **Control Circuit**
- **DC Bus**
- **Output**

**Symbols:**

- $Z_{o,S}$
- $Z_{in,L}$
- $Z_{Bi}$

**Equations:**

$$i_o$$

$$v_o$$
Standard Form of Cascaded System

Small-Signal Two-Port Model

$$\hat{x}_{vj} = G_{BVCCj_1}(s) \hat{x}_{vj} + G_{BVCCj_2}(s) \hat{x}_{vj} + G_{BVCCj_3}(s) \hat{x}_{vj}$$

$$\hat{y}_{vj} = G_{BVCCj_1}(s) \hat{x}_{vj} + G_{BVCCj_2}(s) \hat{x}_{vj} + G_{BVCCj_3}(s) \hat{x}_{vj}$$

$$\hat{x}_{ck} = G_{BCCk_1}(s) \hat{x}_{ck} + G_{BCCk_2}(s) \hat{x}_{ck} + G_{BCCk_3}(s) \hat{x}_{ck}$$

$$\hat{y}_{ck} = G_{BCCk_1}(s) \hat{x}_{ck} + G_{BCCk_2}(s) \hat{x}_{ck} + G_{BCCk_3}(s) \hat{x}_{ck}$$

$$\frac{1}{Z_{c_{busk}}(s)}$$

$$Z_{v_{bus}}$$
Small-Signal Model of Cascaded System

Equivalent Loop Gain of Cascaded System

\[
T_m = \left( \sum_{j=1}^{m} \frac{1}{Z_{v_{busj}}} \right)^{-1}
\]

\[
T_m = \left( \sum_{k=1}^{n} \frac{1}{Z_{i_{busk}}} \right)^{-1}
\]
General Impedance-Based Stability Criterion of Cascaded System

Equivalent Loop Gain of Cascaded System

\[ T_m = \frac{1}{\sum_{j=1}^{m} \frac{1}{Z_{v\_busj}}}^{-1} = \frac{Z_{v\_bus}}{Z_{i\_bus}} \]

- \( Z_{v\_bus} \): Shunt impedance of the bus-side-port-impedances of all the BVCCs.
- \( Z_{i\_bus} \): Shunt impedance of the bus-side-port-impedances of all the BCCCs.

General Impedance-Based Stability Criterion of Cascaded System

- Each converter is stable when working alone;
- \( T_m \) satisfies the Nyquist criterion.
Application of General Impedance-Based Stability Criterion

Equivalent Loop Gain

\[ T_m = \frac{\left( \sum_{j=1}^{m} \frac{1}{Z_{v\_busj}} \right)^{-1}}{\left( \sum_{k=1}^{n} \frac{1}{Z_{i\_busk}} \right)^{-1}} \]

BVCC
- **Source Converter** (Controlling the bus voltage)
- **Load Converter** (Controlling the output voltage/current)

Equivalent loop gain:
\[ T_m = \frac{Z_{o\_S}(s)}{Z_{in\_L}(s)} \]

BCCC
- **Current-Type Grid-Connected Inverter** (Controlling the grid current)
  - **Current-Type Grid-Connected Inverter**

Equivalent loop gain:
\[ T_m = \frac{Z_{in\_g}(s)}{Z_{o\_inv}(s)} \]
Equivalent Loop Gain

\[ T_m = \frac{\left( \sum_{j=1}^{m} \frac{1}{Z_{v_{busj}}} \right)^{-1}}{\left( \sum_{k=1}^{n} \frac{1}{Z_{i_{busk}}} \right)^{-1}} \]

Equivalent loop gain: \[ T_m = \frac{Z_{Bi}(s)}{Z_{o_{s}} // Z_{in_{L}}(s)} \]
**Application of General Impedance-Based Stability Criterion**

**Equivalent Loop Gain**

\[
T_m = \left( \sum_{j=1}^{m} \frac{1}{Z_{v_{busj}}} \right)^{-1} \left( \sum_{k=1}^{n} \frac{1}{Z_{i_{busk}}} \right)^{-1}
\]

**Equivalent loop gain:**

\[
T_m = \left( \sum_{j=1}^{m} \frac{1}{Z_{o_{Sj}}} \right)^{-1} \left( \sum_{k=1}^{n} \frac{1}{Z_{in_{Lk}}} \right)^{-1}
\]
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Input and Output Impedances of Power Converter

**BVCC**

**Source Converter** (Controlling the bus voltage)

- **$f < f_{c_L}$**: $Z_{in\_L} = -V_{bus}^2 / P_o$
- **$f > f_{c_L}$**: $Z_{in\_L}$ behaves as an inductor.

**B CCC**

**Load Converter** (Controlling the output voltage/current)

- **Negative resistor**

**Load Converter**

- At the cut-off frequency $f_{c_S}$, $Z_{o\_s}$ has a resonant peak.
- The magnitude of the resonant peak is inversely proportional to the output filter capacitor.
Analysis of Stability of Cascaded System

Equivalent loop gain: \( T_m = \frac{Z_{o-S}(s)}{Z_{in-L}(s)} \)

- In the entire frequency range, \( Z_{o-S} \) never intersects with \( Z_{in-L} \), i.e., \(|Z_{o-S}| < |Z_{in-L}|\); or
- At the frequency of intersection, \( \angle Z_{o-S} - \angle Z_{in-L} < 180^\circ \).

Unstable!
Improving the Stability of Cascaded System

BVCC

Source Converter
(Controlling the bus voltage)

\[ V_{bus} \]

\[ i_{in} \]

\[ V_{in} \]

\[ - \]

Load Converter
(Controlling the output voltage/current)

\[ V_{o} \]

\[ i_{o} \]

Introduce a virtual impedance \( Z_{vir} \) at the bus-side of load converter

Equivalent loop gain:

\[ T_m = \frac{Z_{o-S}(s)}{Z_{in-L}(s)} \]

\( T_m \) satisfied Nyquist criterion

- In the entire frequency range, \( Z_{o-S} \) never intersects with \( Z_{in-L} \), i.e., \( |Z_{o-S}| < |Z_{in-L}| \); or
- At the frequency of intersection, \( \angle Z_{o-S} - \angle Z_{in-L} < 180^\circ \).

Increase the magnitude of \( Z_{in-L} \) in the vicinity of \( f_{c_S} \)

Increase the phase of \( Z_{in-L} \) in the vicinity of \( f_{c_S} \)

Load is reduced

幅值 (dB)

相位 (°)

In the entire frequency range, \( Z_{o-S} \) never intersects with \( Z_{in-L} \), i.e., \( |Z_{o-S}| < |Z_{in-L}| \); or

At the frequency of intersection, \( \angle Z_{o-S} - \angle Z_{in-L} < 180^\circ \).
Introduce Virtual Impedance for Regulating $Z_{in_L}$

- **Parallel Virtual Impedance (PVI)**
  - BVCC
    - Source Converter (Controlling the bus voltage)
    - BCCC
      - Load Converter (Controlling the output voltage/current)

- **Series Virtual Impedance (SVI)**
  - BVCC
    - Source Converter (Controlling the bus voltage)
  - BCCC
    - Load Converter (Controlling the output voltage/current)
Realization of Parallel Virtual Impedance

**BVCC**
- Source Converter (Controlling the bus voltage)
- \( V_{bus} \) to \( i_{in} \)
- \( V_{in} \)

**BCCC**
- Load Converter (Controlling the output voltage/current)
- \( V_o \) to \( i_o \)

**Basic idea**
- \( Z_{in} \)
- \( Z_{vir} \)

**Realization**
- \( G_{v}(s) \) to \( \hat{V}_{o\_ref} \)
- \( G_{PWM}(s) \) to \( \hat{d} \)
- \( G_{vn}(s) \) to \( \hat{V}_{e} \)
- \( G_{vd\_OL}(s) \) to \( \hat{V}_{o} \)
Realization of Series Virtual Impedance

Source Converter (Controlling the bus voltage)

Load Converter (Controlling the output voltage/current)

**BVCC**

- $i_{in}$
- $V_{in}$
- $V_{bus}$
- $i_{in,L}$
- $Z_{vir,S}$
- $Z_{o,S}$
- $Z_{in,L}$
- $Z_{in,L_ori}$

**BCCC**

- $i_o$
- $V_o$

---

**Basic idea**

**Realization**

$G_{zin,S}$

$Z_{vir,S}(s)$

$G_{PWM}(s)$

$H_s(s)$

$G_{v_{d,OL}}(s)$

$G_{v_{g,OL}}(s)$

$G_{i_d,OL}(s)$

$G_{i_i,OL}(s)$

$Z_{o,OL}(s)$

$Z_{in,OL}(s)$

$1$
Prototype

**Source Stage**

- **Input voltage** $V_{in}$: 48 VDC
- **Output voltage** $V_o$: 12 VDC
- **Rated output power** $P_o$: 100 W
- **Input filter inductor** $L_{f1}$: 700 $\mu$H
- **Input filter capacitor** $C_{f1}$: 68 $\mu$F
- **Output filter inductor** $L_{f2}$: 33 $\mu$H
- **Output filter capacitor** $C_{f2}$: 2400 $\mu$F
- **Switching frequency** $f_s$: 100 kHz

**Load Converter**

**Note:**
- $QL$, $Lf2$, $Cf2$, $R_{ld}$
- $D_{FW}$
- $v_{bus}$, $i_{in}$
- $v_o$, $RLd$, $RLf$, $Vin$, $Z_{in\_L}$, $Z_{o\_S}$
Input and Output Impedances with PVI

\[ f_1 = 685 \text{ Hz} \]
\[ f_2 = 780 \text{ Hz} \]
Experimental Waveforms

<table>
<thead>
<tr>
<th></th>
<th>W/O parallel virtual impedance</th>
<th>With parallel virtual impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Full Load</strong></td>
<td><img src="image1" alt="Waveform" /></td>
<td><img src="image2" alt="Waveform" /></td>
</tr>
<tr>
<td><strong>Half Load</strong></td>
<td><img src="image3" alt="Waveform" /></td>
<td><img src="image4" alt="Waveform" /></td>
</tr>
<tr>
<td><strong>35% Full Load</strong></td>
<td><img src="image5" alt="Waveform" /></td>
<td><img src="image6" alt="Waveform" /></td>
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</tbody>
</table>
Dynamic Response with PVI

The load is stepped change

The input voltage is stepped changed
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Adaptive Impedance Adaptor: Basic Concept

Reduce the magnitude of the BVCC’s bus-side port impedance, and it is adaptively vary with the load, ensuring the cascaded system stable critically.

Add a capacitor in parallel with the dc bus
The capacitance adaptively vary with the load.

Propose an active capacitor converter, and the emulated capacitor is required to vary with the load.
Adaptive Impedance Adaptor: Circuits Implementation and Control Method

Source Converter (Controlling the bus voltage)

Bus Ripple Voltage Regulator

Differential Circuit

Multiplier

DC-side Capacitor Voltage Regulator

Current Regulator

PWM Modulator

High-pass filter

Impedance Adaptor

Bus Converter (Controlling the bus voltage)

Load Converter (Controlling the output voltage/current)
Adaptive Impedance Adaptor: Prototype

Source Converter (Full-Bridge)
- Winding ratio of transformer: 5
- Filter inductor $L_{f1}$: 150 $\mu$H
- Filter capacitor $C_{f1}$: 680 $\mu$F

Load Converter (Full-Bridge)
- Winding ratio of transformer: 3
- Filter inductor $L_{f2}$: 2.2 $\mu$H
- Filter capacitor $C_{f2}$: 4700 $\mu$F

Impedance Adaptor (Buck/Boost)
- Inductor $L_a$: 395 $\mu$H
- DC-side capacitor $C_a$: 20 $\mu$F

360V $V_{in}$ $i_{in}$ Full-Bridge Converter

48V $V_{bus}$ $i_{in_L}$ Full-Bridge Converter

12V/40A $V_o$ $i_o$ BVCC

Impedance Adaptor

Source Converter

Load Converter

Impedance Adaptor
Output Impedance of Source Converter and Input Impedance of Load Converter

- At higher than 35% full-load, $Z_{o_s}$ intersects with $Z_{in_L}$. This means that the cascaded system is **unstable**.

- At lower than 35% full-load, $Z_{o_s}$ does not intersect with $Z_{in_L}$. This means that the cascaded system is **stable**.
The impedance adaptor is not required to operate, and it is shut down.
Fast dynamic response!

With 1950\(\mu\)F Electrolytic capacitor

With the impedance adaptor
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Conclusions

- The concept of bus voltage controlled converter (BVCC) and bus current controlled converter (BCCC) is proposed, and any converter in the cascaded system can be classified as either a BVCC or a BCCC, thus a cascaded system can be represented in a general form regardless of its structure and operating mode.

- The general impedance-based stability criterion for cascaded system is proposed, and the equivalent loop gain is equal to the ratio of the shunt impedance of the bus-side-port-impedances of all the BVCCs and the bus-side-port-impedances of all the BCCCs.

- Regarding the load converter, which is a BCCC, a method of regulating the input impedance based on virtual impedance is proposed, which increases the magnitude or phase of the input impedance in the vicinity of the intersection frequency, thus ensuring the cascaded system stable.

- The adaptive impedance adaptor is proposed, which emulates a capacitor connected in parallel with the dc bus. This emulated capacitor varies adaptively with the load, and avoiding the impedance intersection over the full frequency range, ensuring the cascaded system stable. The adaptive impedance adaptor has the advantages of fast dynamic response compared with the passive capacitor and modular design without any information of the converters in the system.
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Thank you very much for Your attention!